REMARKS

Claims 1-15 were pending in the application. In response to the Office Action, applicants have amended the specification and added new claims 16-22. Claims 1-22 are now pending for reconsideration.

The changes to the specification are set forth in the attachment entitled VERSION WITH MARKINGS TO SHOW CHANGES MADE, with ~~strikethrough~~ indicating deletions and underlining indicating additions.

The specification has been amended editorially. No new matter has been added.

Claims 1-7 and 14-15 were rejected under 35 U.S.C. § 102(b) as being anticipated by Thantrakul (U.S. Patent No. 5,784,611). Claims 8-13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Thantrakul. Applicants respectfully traverse these rejections for the following reasons.

Each of independent claims 1, 8 and 14 recite communication between a CPU and a firmware hub module via a low pin count (LPC) bus. Thantrakul fails to teach or suggest this claim feature.

In order to anticipate, the reference must identically disclose the claimed invention. Thantrakul does not even mention a firmware hub or an LPC bus. As noted in the specification, an LPC bus generally includes general purpose signal lines that carry substantially all time-multiplexed address, data and control information to implement memory, I/O, and bus transactions between the CPU and other system devices. In contrast, Thantrakul discloses only the conventional bus arrangement with separate, address, data, and control lines. Because the recited low pin count bus is different from the buses disclosed in Thantrakul, independent claims 1 and 14, and their dependent claims 2-7 and 15, respectively, are not anticipated by Thantrakul.

Moreover, the claimed firmware hub recovery for a LPC bus is patentably distinct over the system disclosed in Thantrakul. As noted in the specification, conventional bus arrangements require a high pin count, with a corresponding increases in cost and complexity. The LPC bus reduces pin count and accordingly provides advantages not taught or suggested by Thantrakul.

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In fact, Thantrakul teaches away from the claimed invention. Thantrakul teaches that the disclosed in-system programmer module requires at least two and preferably at least four dedicated signal lines connected between the module and the CPU control logic in addition to the normal bus lines (see signal lines 30, 32, 52, and 54 in Fig. 2). For example, in connection with Fig. 1, Thantrakul discloses, the "interface between the control logic 28 and the memory module 26 requires two extra signal lines 30 and 32 above normal microprocessor bus 22 interface signals." (see col. 5, lines 17-20, emphasis added). Thantrakul thus teaches to increase the pin count above the normal bus pin count, which is contrary to the claimed invention.

Because Thantrakul fails to teach or suggest the recited communication between a CPU and a firmware hub module via a low pin count (LPC) bus, independent claims 1, 8, and 14 are patentable over Thantrakul. Claims 2-7 depend from claim and are likewise patentable. Claim 9-13 depend from claim 8 and are likewise patentable. Claim 15 depends from claim 14 and is likewise patentable.

Applicant has presented new dependent claims 16-22 which further define the invention and are believed to be patentable.

Each of claims 16, 18, and 21 recite that the CPU communicates with the firmware hub recovery module only via the LPC bus. As noted above, this feature is patentably distinct over Thantrakul which requires dedicated lines outside of the normal bus lines.

Each of claims 17, 19, and 22 recite that the firmware hub module is responsive as the booting firmware hub in accordance with an identification sent from the CPU. This feature is patentably distinct from Thantrakul in which the module sends an "in-system programmer attached" (ISPA) signal to the CPU to indicate the presence of the module (see col. 6, lines 6-11) over one of the dedicated signal lines.
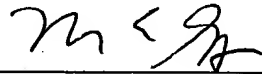
Claim 20 is directed to the structural features not taught or suggested by Thantrakul.

In view of the foregoing, favorable reconsideration and withdrawal of the rejections is respectfully requested. Early notification of the same is earnestly solicited. If there are any questions regarding the present application, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

January 21, 2003
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

The paragraph on page 1, lines 20-25 is amended as follows:

--   The large number of pins needed to support the ISA bus and X-bus standards generally increase the overall system cost. For example, larger packages are required for a CPU or chip-set. The development of the low pin count (LPC) bus has obviated to some extent the problem mentioned above. The LPC bus includes general purpose signal lines ~~the~~ that carry substantially all time-multiplexed address, data and control information to implement memory, I/O, and bus transactions between the CPU and other system devices.   --

The paragraph on page 4, lines 4-18 is amended as follows:

--   FIG. 1 illustrates a block diagram of a computer system's circuit board 27 including a low pin count (LPC) bus 39 according to an embodiment of the present invention.   Circuit board 27 may be a mother board and typically includes a processor such as a central processing unit or CPU 20. The CPU is the "brains" or "engine" of the computer system responsible for overseeing all execution of operations in the computer. Motherboard 27 also includes CPU interface logic 21, coupled to CPU 20 and interfacing CPU 20 with other circuit components such as a system bus interface controller 33 and main memory 26. As shown, system bus interface controller 33 may be any type of expansion bus controller such as a PCI bus or peripheral bus I/O controller. System bus interface controller 33 is coupled to CPU interface logic 21 and is coupled to peripheral connectors 25 via expansion bus 38.   A bus ~~the~~ that complies with a Peripheral Component Interconnect (PCI) standard (e.g., PCI Local Bus Specification, version 2.1, a copy of which may be obtained from the PCI Special Interest Group) is a example of such an expansion bus.   Main memory 26 may include random access memory (RAM) 28 and read only memory (ROM) 30 which coupled to CPU interface logic 21.   --

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